REMARKS

Applicant respectfully requests further examination and reconsideration in view of th instant amendment and response. Claims 1-18, 30 and 31 remain pending in the case. Claims 1-18, 30 and 31 are rejected. Claims 1, 9, 15 and 17 are cancelled herein without prejudice. Claims 2, 4-8, 10-14, 16, 18, 30 and 31 are amended herein. No new matter has been added.

Examiner Telephone Conference

On May 28, 2003, Examiner Ortiz telephone Mr. Blecher regarding the status of non-elected Claims 19-29. Specifically, Examiner Ortiz indicated that new patent practice requires a status identifier to accompany each claim of the application, even those that are no longer pending. The current Supplemental Amendment and Response now indicates that Claims 19-29 are directed towards non-elected subject matter and have been withdrawn.

35 U.S.C. §102(e)

Claims 2-8, 10-14, 16, 18, 30 and 31 stand rejected under 35 U.S.C. §102(e) as being anticipated by United States Patent 6,262,453 by Hshieh, hereinafter referred to as the "Hshieh" reference. Applicants have reviewed the cited reference and respectfully submit that the embodiments of the present invention as recited in Claims 2-8, 10-14, 16, 18, 30 and 31 are not anticipated by Hshieh.

Applicant respectfully dir cts the Examiner to indep ndent Claim 4 that r cites that an mbodiment of th present invention is direct d to (emphasis added):

> A metal-insulator-semiconductor (MIS) device, comprising:
> a semiconductor substrate defining a trench extending into said substrate from a surface of said substrate;
> a source region of a first conductivity type adjacent to a sidewall of said trench and to said surface;
> a body region of a second conductivity type opposite to said first conductivity type adjacent to said source region and to said sidewall;
>
> a drain region of said first conductivity type adjacent to said body region and to said sidewall;
> wherein said trench is lined with a first insulative layer along a portion of said sidewall that abuts said body region and wherein said trench is lined with a second deposited insulated layer along said bottom portion of said trench, said second insulative layer being in contact with said first insulative layer, whereby formation of said second insulative layer does not introduce substantial stress in said substrate; and
> a high conductivity region of said first conductivity type in said drain region adjacent to at least said bottom portion of said trench.

Independent Claims 11, 16 and 18 recite similar limitations. Claims 2, 3, 5-8 and 30 that depend from independent Claim 4 and Claims 10, 12-15 and 31 that depend from independent Claim 11 provide further recitations of features of the present invention.

Hshieh and the claimed invention are very different. Applicants understand Hshieh to teach a DMOS transistor having a double gate-oxide for reducing gate-drain capacitance. In particular, Hshieh teaches a high-dopant

concentration buried-region under a trenched gat of the DMOS transistor. The high-dopant concentration is buried und r th bottom of the trench, and is not adjacent to the trench or the trenched gate.

In contrast, embodiments of the claimed invention are directed toward a metal-insulator-semiconductor (MIS) device comprising a high conductivity region of a first conductivity type in the drain region adjacent to at least the bottom portion of the trench. In particular, the high conductivity region is in direct contact with the bottom portion of the trench. As shown in Figure 5 of the current application, a high-doping region 53 is located at the bottom of trench 19 to help spread current more effectively. High-doping region 53 is in direct contact with the bottom of trench 19, and is insulated from gate 14 by thick insulative layer 31. Thick insulative layer 31 minimizes gate-to-drain capacitance and high-doping region 53 minimizes on-resistance, yielding a trench MOSFET 50 well-suited for use in high frequency application (see page 7, lines 13-20 of the current application.

Applicant respectfully asserts that Hshieh in particular does not teach, disclose, or suggest a MIS device comprising a high conductivity region of a first conductivity type in the drain region adjacent to at least the bottom portion of the trench, as claimed. In contrast, Hshieh discloses a DMOS transistor having a high-dopant concentration buried-region under a trenched gate of the DMOS transistor.

The Hshieh transistor 100 has a high-dopant concentration N+ buried region 118 formed blow the bottom of trench 125 (see Hshieh, Figure 2A and col. 4, lines 65-67). "A high-dopant-concentration N+ buried region 118 is formed underneath the bottom of each trench 115" (emphasis added, see Hshieh, Figure 3B and col. 5, lines 40-41. In particular, Hshieh teaches that there is no significant increase of the gate-to-drain capacitance because the dopant concentration near the bottom of trenched gate 125 is not significantly increased (col. 5, lines 5-9). In contrast, embodiments of the present invention are directed towards minimizing the gate-to-drain by increasing the dopant concentration at the bottom of a trenched gate. Hshieh does not teach, disclose, or suggest a MIS device comprising a high conductivity region of a first conductivity type in the drain region adjacent to at least the bottom portion of the trench, as claimed. On the contrary, Hshieh teaches away from such a configuration, as the drain region of Hshieh comprises high doping concentration buried beneath the trenched gate.

Applicants respectfully assert that nowhere does Hshieh teach, disclose or suggest the present invention as recited in independent Claims 4, 11, 16 and 18, and that these claims are not anticipated or rendered obvious by the cited reference. Therefore, Applicants respectfully submit that Hshieh also does not teach or suggest the additional claimed features of the present invention as recited in Claims 2, 3, 5-8 and 30 that depend from independent

Claim 4 and Claims 10, 12-15 and 31 that depend from indep ndent Claim 11. Therefore, Applicants respectfully submit that Claims 2, 3, 5-8, 10, 12-15, 30 and 31 overcome the rejection under 35 U.S.C. § 102(b), and are in condition for allowance as being dependent on an allowable base claim.

CONCLUSION

Based on the amendments presented above, Applicants resp ctfully assert that Claims 2-8, 10-14, 16, 18, 30 and 31 are allowable and, therefore, Applicants respectfully solicit allowance of these Claims.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

WAGNER, MURABITO & HAO L.L.P.

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Matthew J. Blecher
Registration No. 46,558

Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060